

MODEL : 8889

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Revision 02

POWER STATES

STATE SIGNAL	VOTAGE	POWER ON	STR (S3)	STD (S4)	MEC-OFF (S5)	REMARK
SUSB#	-	HIGH	LOW	LOW	LOW	
SUSC#	-	HIGH	HIGH	LOW	LOW	
ADP	+19V	0	0	0	0	
BATTERY	+12V	0	0	0	0	
+5VA	+5V	0	0	0	0	
+3VA	+3.3V	0	0	0	0	
+5VSB	+5V	0	0	0	X	
+3VSB	+3.3V	0	0	0	X	
+5V	+5V	0	0	X	X	
+3V	+3.3V	0	0	X	X	
+2.5V	+2.5V	0	0	X	X	
+1.25V	+1.25V	0	0	X	X	
+5VS	+5V	0	X	X	X	
+3VS	+3.3V	0	X	X	X	
+2.5VS	+2.5V	0	X	X	X	
+2.5VDDA	+2.5V	0	X	X	X	
+1.5VS	+1.5V	0	X	X	X	
+1.2VLDTA	+1.2V	0	X	X	X	
+CPU_CORE	+1.2V	0	X	X	X	

IDSEL

IDSEL	CHIP
AD20	CardBus
AD21	MiniPCI

I2C / SMB Address

DEVICE	WRITE ADDRESS	READ ADDRESS
CLK GEN	D2	D3
DIMM0	A0	A1
DIMM1	A2	A3
G781	98	99

BUS MASTER

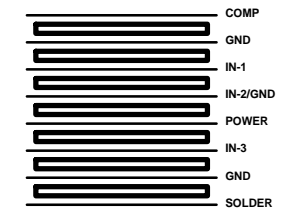
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-REQ0/-GNT0	CardBus
-REQ1/-GNT1	
-REQ2/-GNT2	MINI PCI
-REQ3/-GNT3	

PCIINT

PCIINT	CHIP
INTA#	VGA
INTB#	CardBus
INTC#	MiniPCI
INTD#	MiniPCI
INTE#	

+3VA	VT8235 W83L950D	5uA 20mA
+CPU_CORE	CPU	30A
+5V	USB PORT * 4 MIMIPCI	2A 300mA
+5VS	CP2211 CRT HDD ODD MINIPCI MDC TPA0212 ALC655	1A 1A 1.5A 1.8A 100mA 500mA 1A 50mA
+3VSB	VT8235	160mA
+3V	CB1410 VT6103L MIMIPCI	200mA 130mA 380mA
+3VS	CP2211 K8N800 CLK_GEN LCDVCC VT8235 CB1410 ALC655 LPC BIOS ROM VT6103L MIMIPCI W83L950D	1A 400mA 360mA 1A 15mA 15mA 200mA 15mA 10mA 430mA 20mA
+2.5VSB	VT8235	6mA
+2.5V	CPU DDR_DIMM	3A 4A
+2.5VS	VT8235 VT1634	400mA 44mA
+1.5VS	K8N800	1A
+1.25V	DDR_DIMM	1A
+1.2VLDT	K8N800 CPU	200mA 500mA

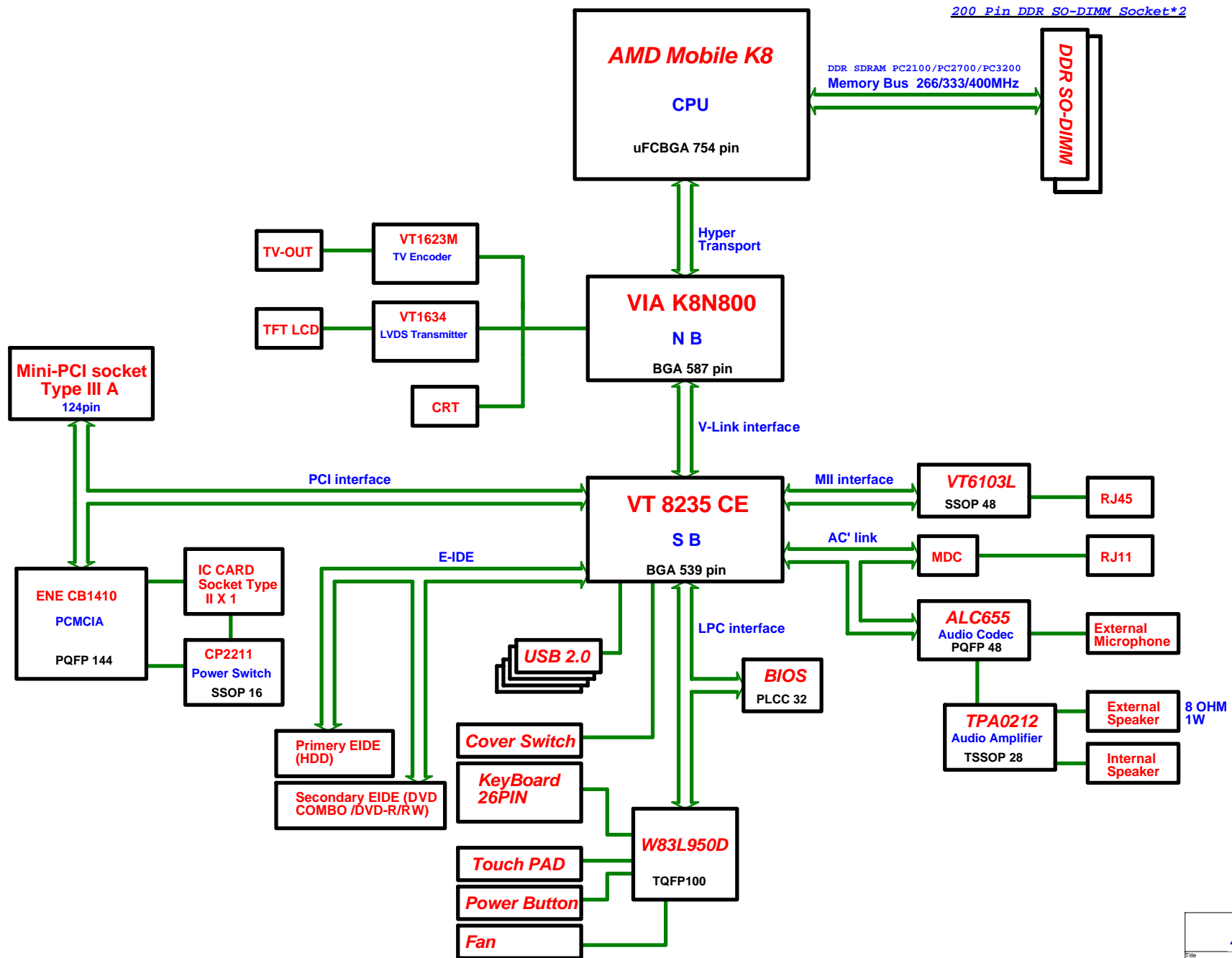
Board Stackup-up



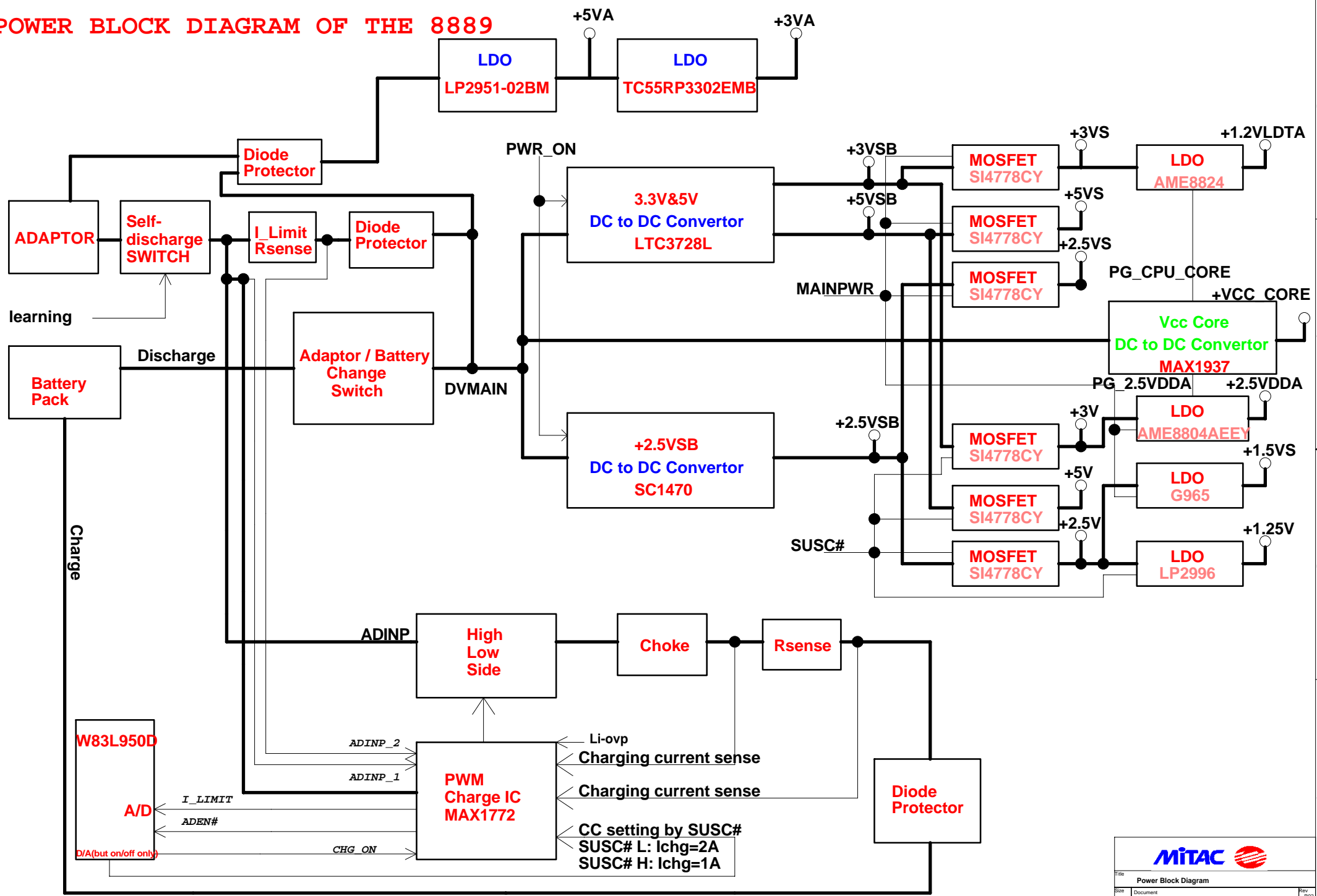
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Date: Monday, August 24, 2004	Sheet: 1	of 30

8889 SYSTEM BLOCK DIAGRAM



POWER BLOCK DIAGRAM OF THE 8889

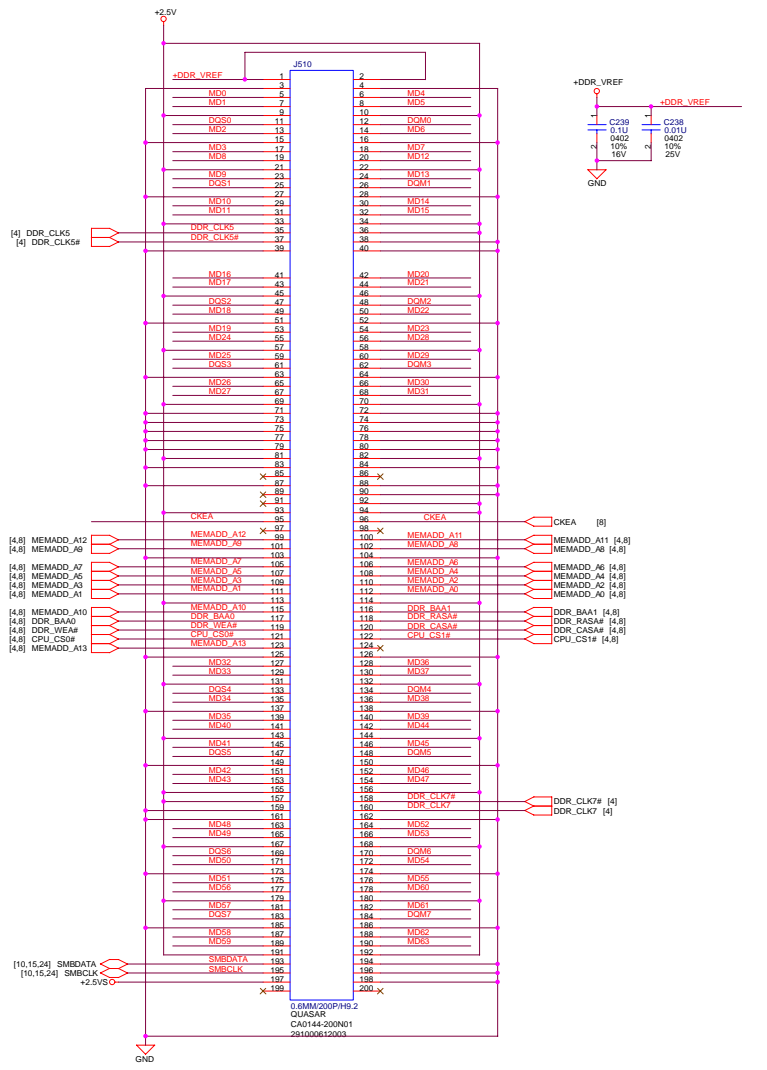


DDR_SODIMM(1/2)

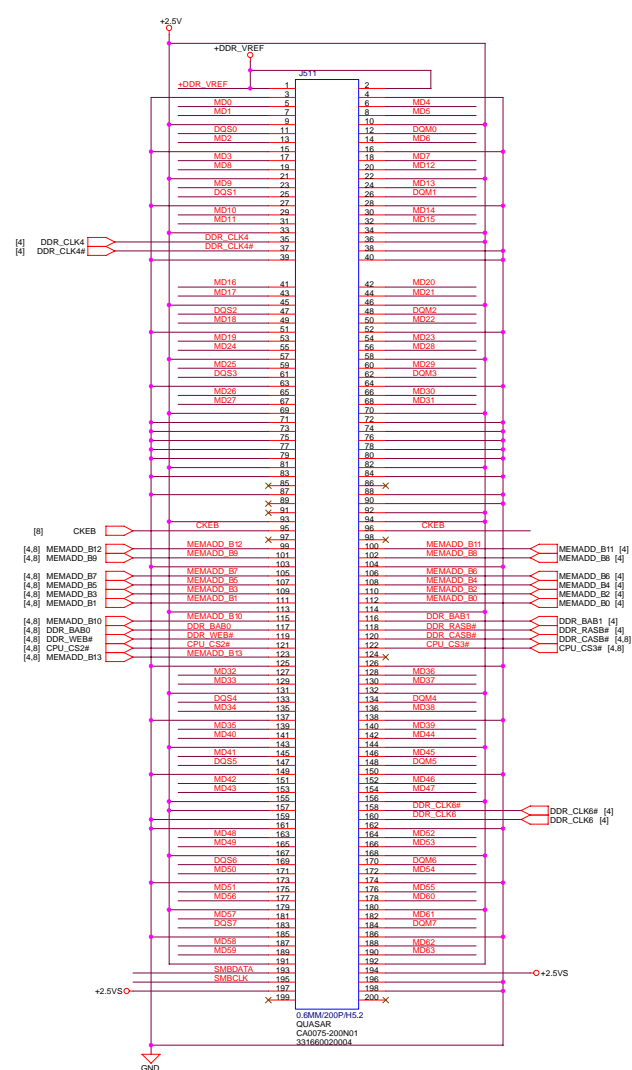
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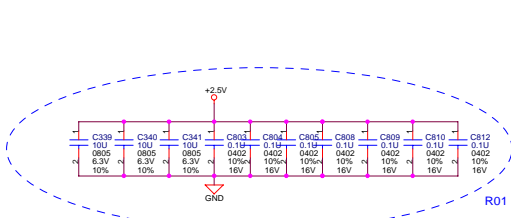
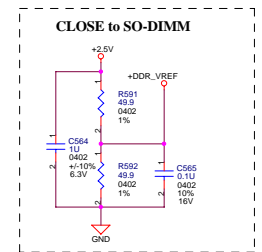
DDR_SODIMM (2 / 2)



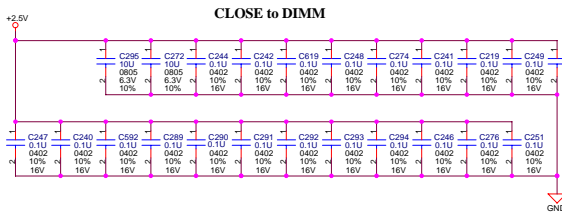
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I2C / SMB Address : A2h



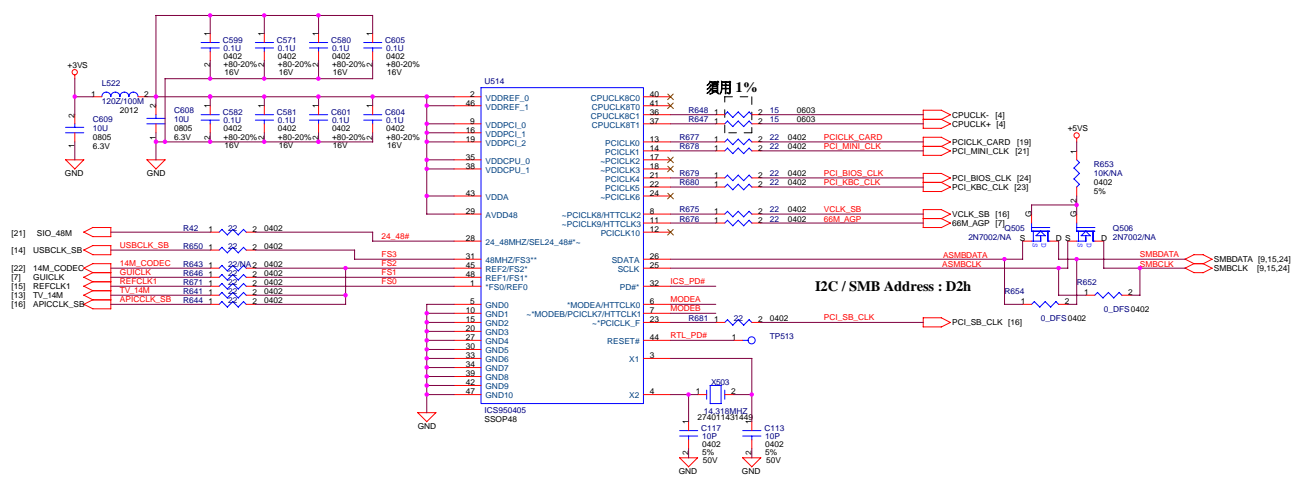
R01



CLOSE to DIMM

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 Date: Monday, August 23, 2004
 Sheet: 9 of 30

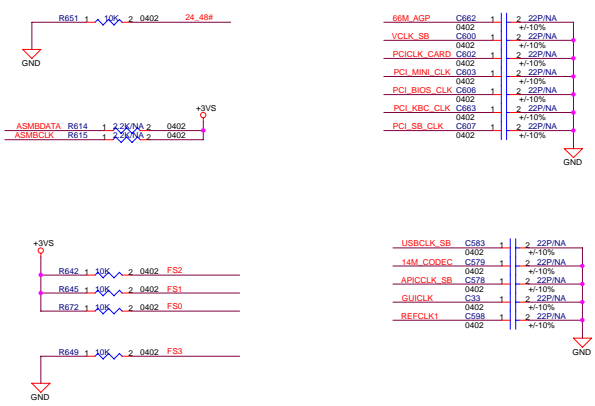
CLOCK GENERATOR(ICS950405)



MODE FUNCTIONALITY TABLES

MODE A	MODE B	Pin6	Pin7	Pin8	Pin11
0	0	66MHz	66MHz	66MHz	33MHz
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1	0	33MHz	33MHz	33MHz	33MHz
1	1	MODE A INPUT ONLY	33MHz	33MHz	33MHz

DEFAULT

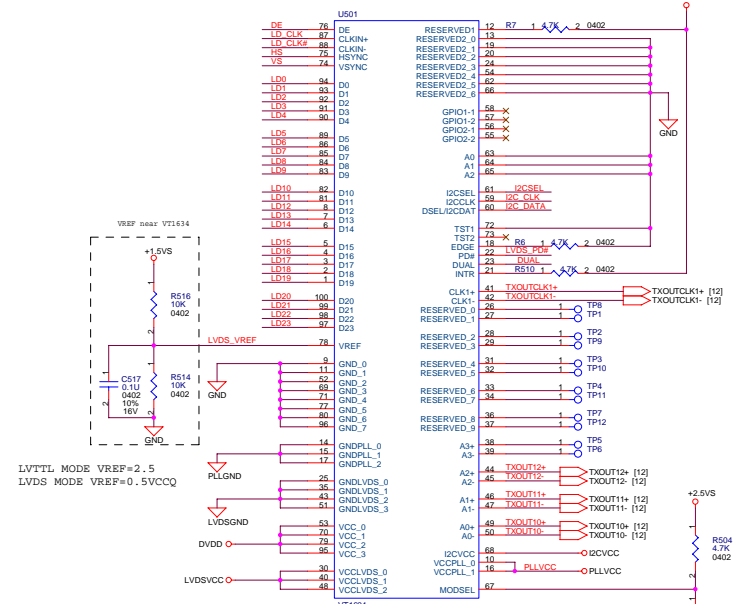
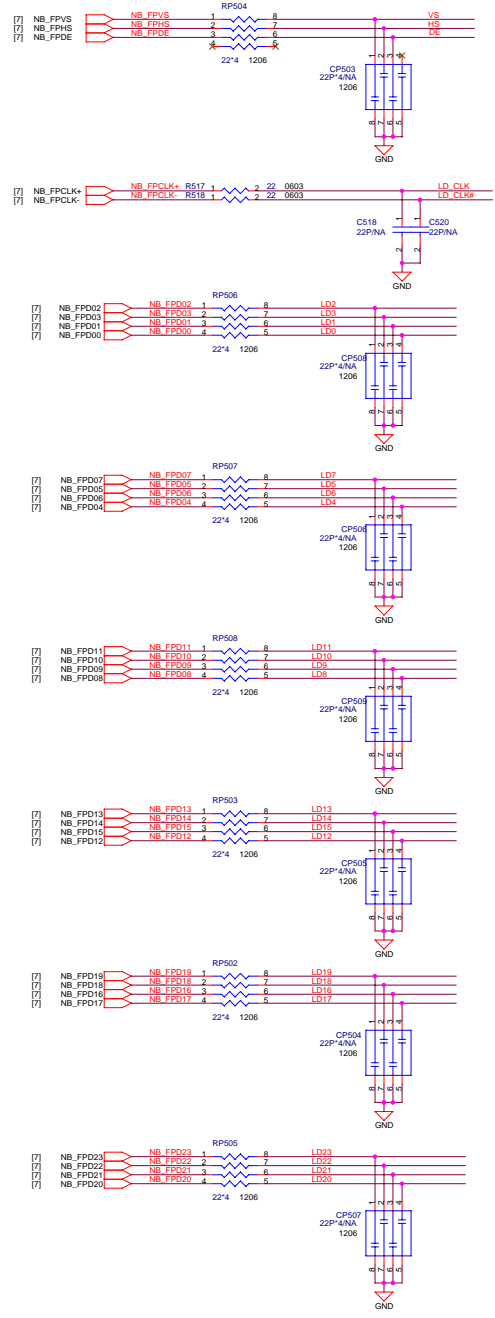


FS3	FS2	FS1	FS0	CPU Mhz	HTT Mhz	PCI Mhz
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0	0	1	0	168.00	67.20	33.60
0	0	1	1	202.00	67.33	33.67
0	1	0	0	100.20	66.80	33.40
0	1	0	1	133.50	66.75	33.38
0	1	1	0	166.70	67.68	33.34
0	1	1	1	200.00	67.80	33.40
1	0	0	0	150.00	60.00	33.00
1	0	0	1	180.00	60.00	33.00
1	0	1	0	210.00	70.00	35.00
1	0	1	1	240.00	60.00	33.00
1	1	0	0	270.00	67.50	33.75
1	1	0	1	233.33	66.67	33.33
1	1	1	0	266.67	66.67	33.33
1	1	1	1	300.00	75.00	37.50

DEFAULT

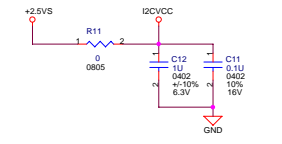
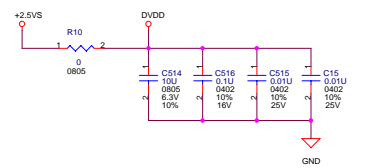
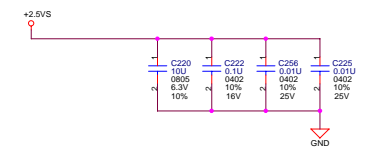
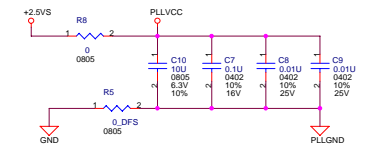
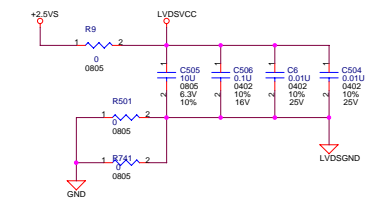
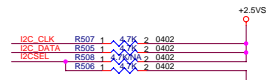
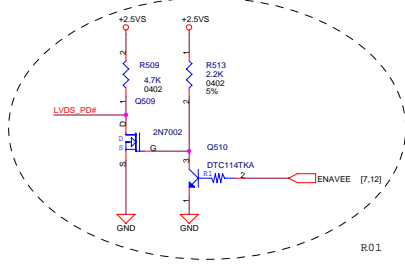
Title: Clock Generator
 Size: 10 of 30
 Date: Monday, August 23, 2004
 Document Number: 316685200002
 Rev: R02

VT1634 LVDS Transmitter



LVTTTL MODE VREF=2.5
LVDS MODE VREF=0.5VCCQ

1 : Dual Channel
0 : One Channel



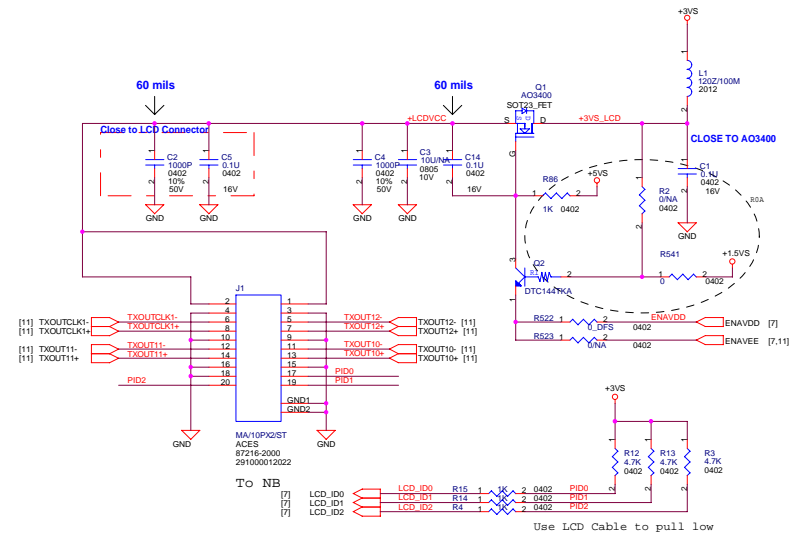
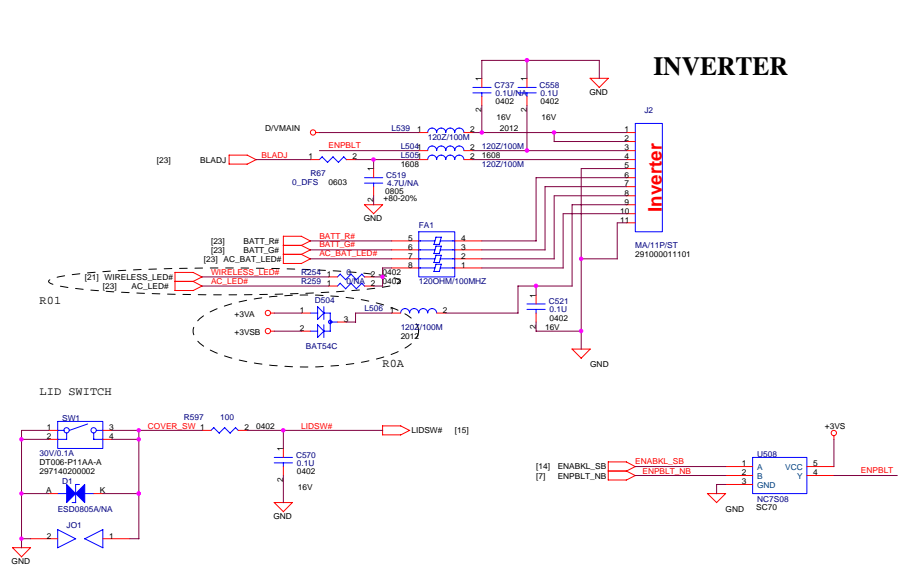
MITAC logo and document information:

Title: LVDS Transmitter VT1634
 Size: 116685200002
 Document Number: 316685200002
 Date: Monday, August 23, 2004
 Sheet: 11 of 30

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Display (CRT / LCD)

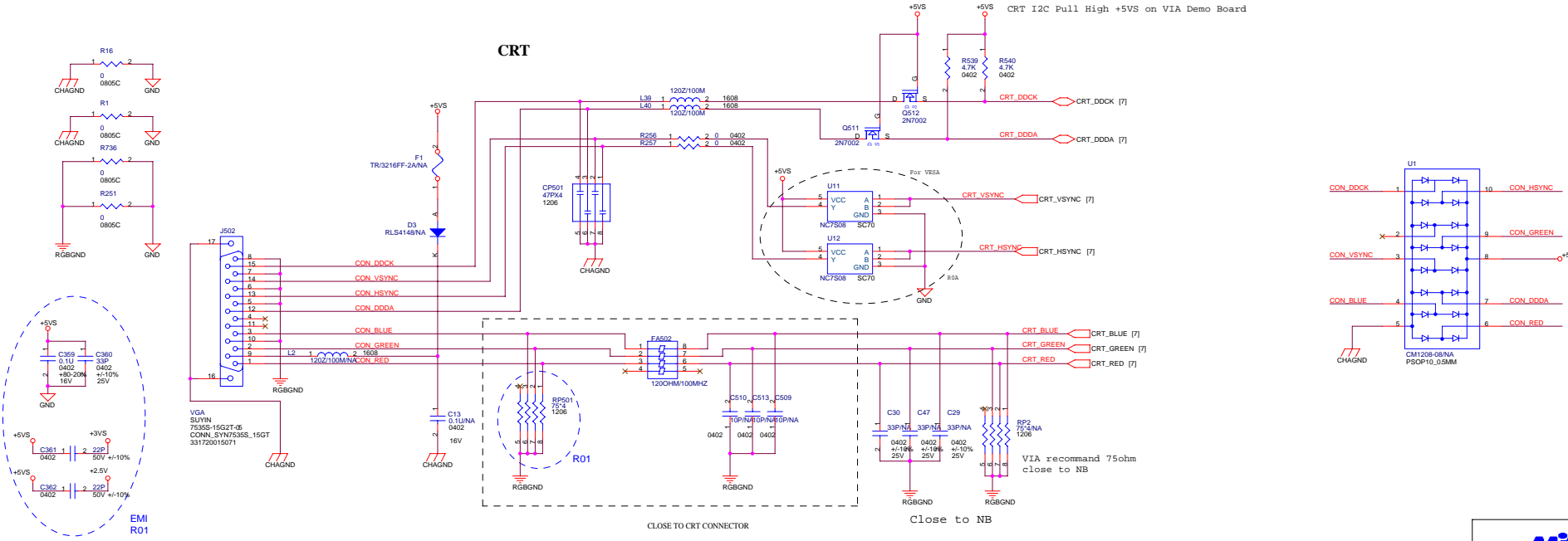
INVERTER



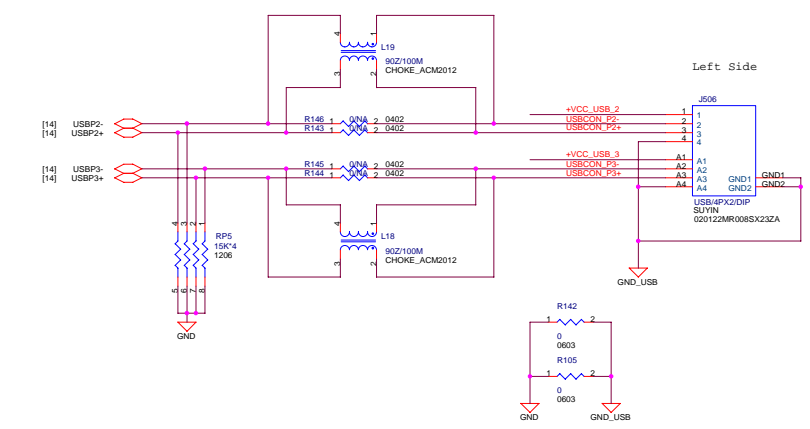
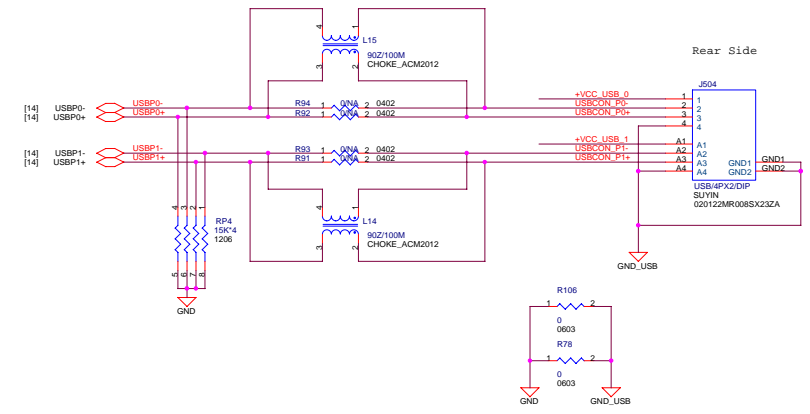
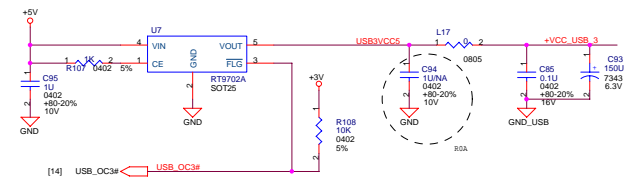
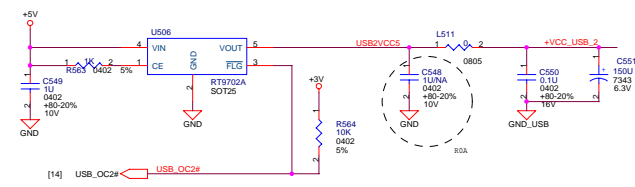
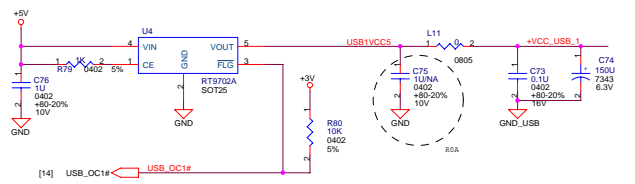
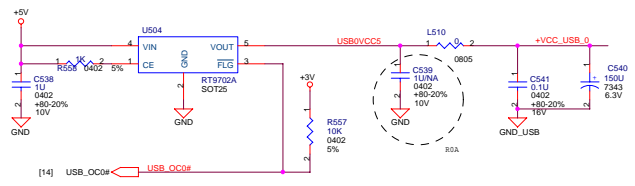
LCD Panel ID

LCD_ID2	LCD_ID1	LCD_ID0	PANEL TYPE
X	X	X	Samsung 15" ETN150XB-L03
X	X	X	Hydix 15" HTL5X34
X	X	X	Hannstar 15" HSD150PX14A
X	X	X	Topoly 14" TD141TCGB1

CRT

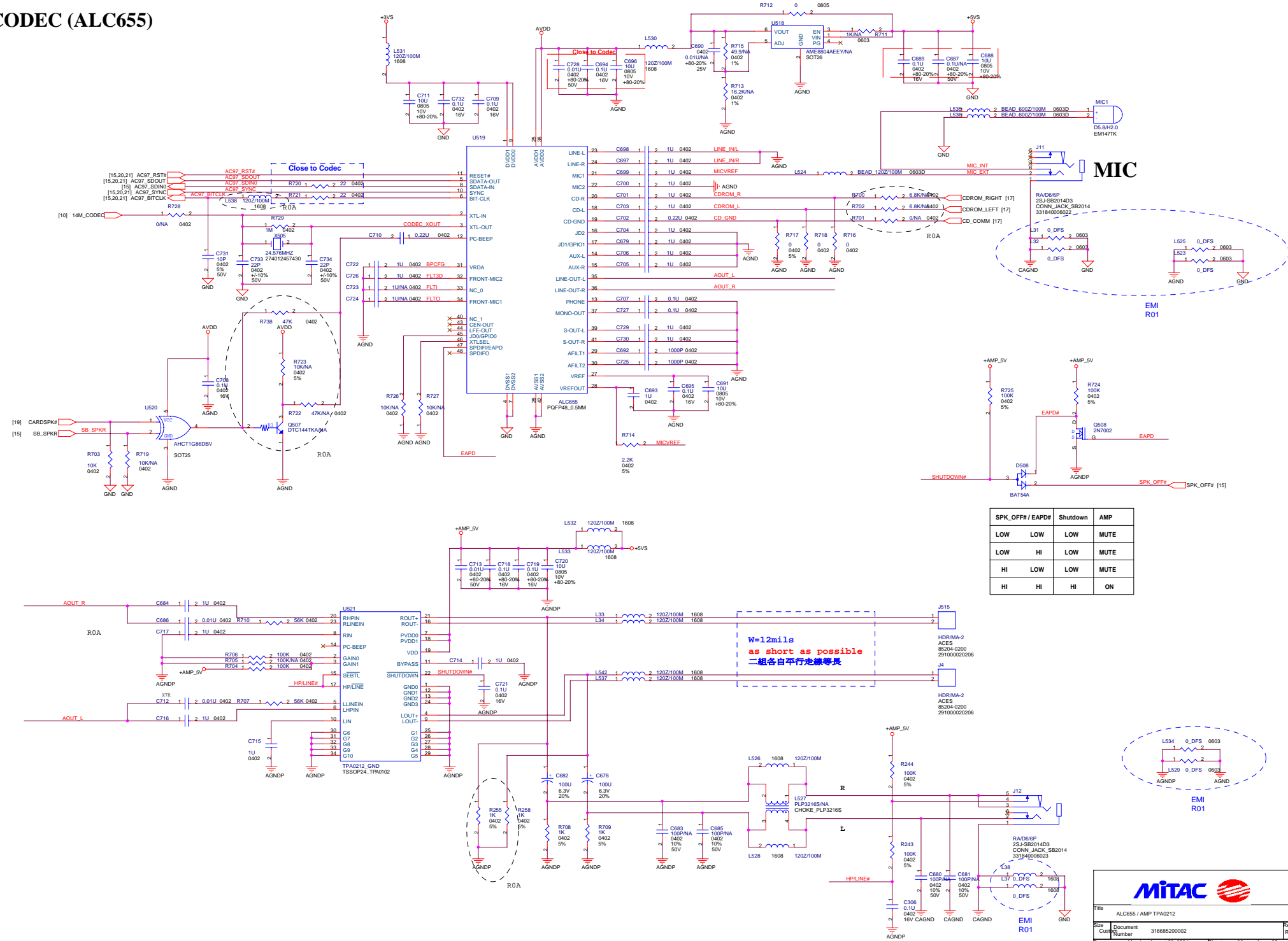


USB CONNECOTR



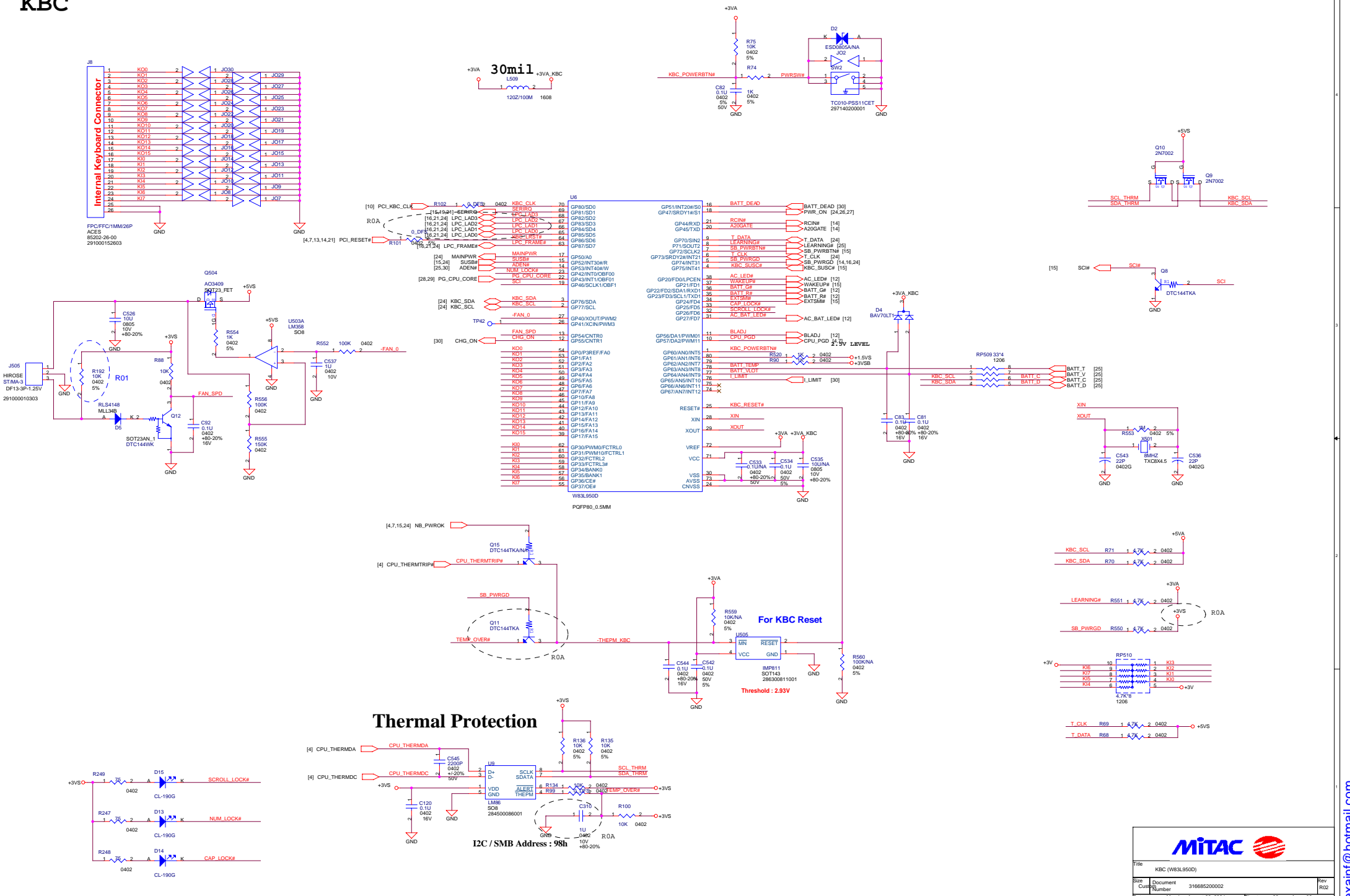
Title		USB
Size	Document	316685200002
Quantity	Number	
Date	Monday, August 23, 2004	Sheet 18 of 30
Rev	R02	

Audio CODEC (ALC655)

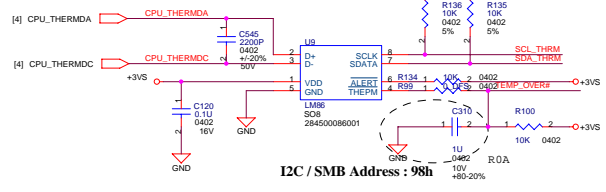


SPK_OFF# / EAPD#	Shutdown	AMP
LOW	LOW	MUTE
LOW	HI	MUTE
HI	LOW	MUTE
HI	HI	ON

File: ALC655 / AMP TPA0212
 Size: 31688520002
 Date: Monday, August 23, 2004 Sheet 22 of 30



Thermal Protection



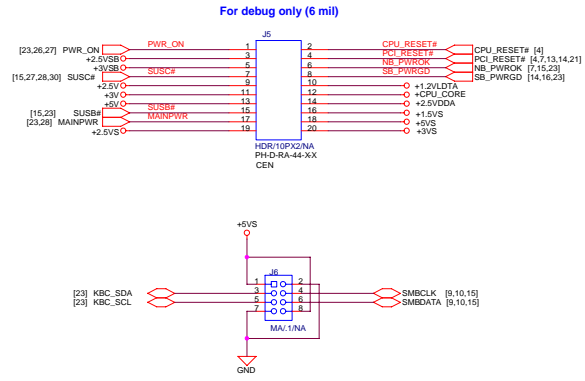
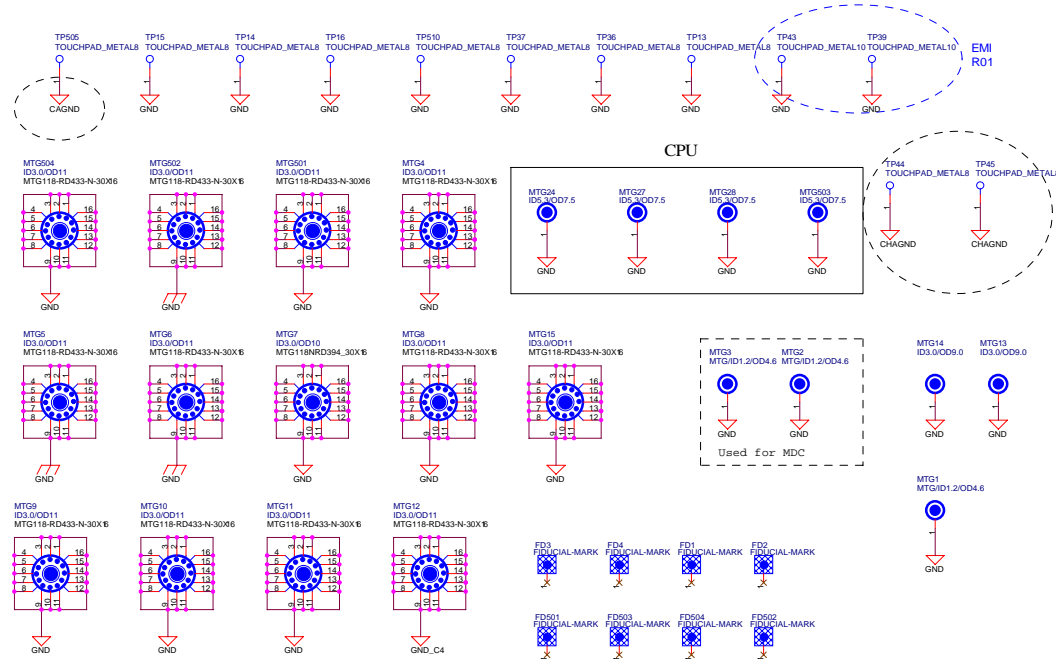
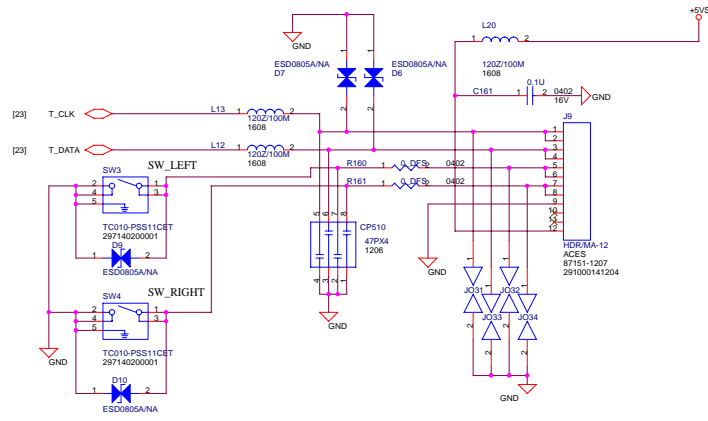
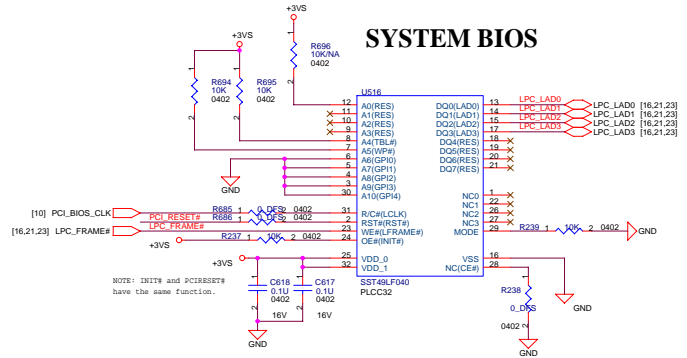
12C / SMB Address : 98h

MITAC

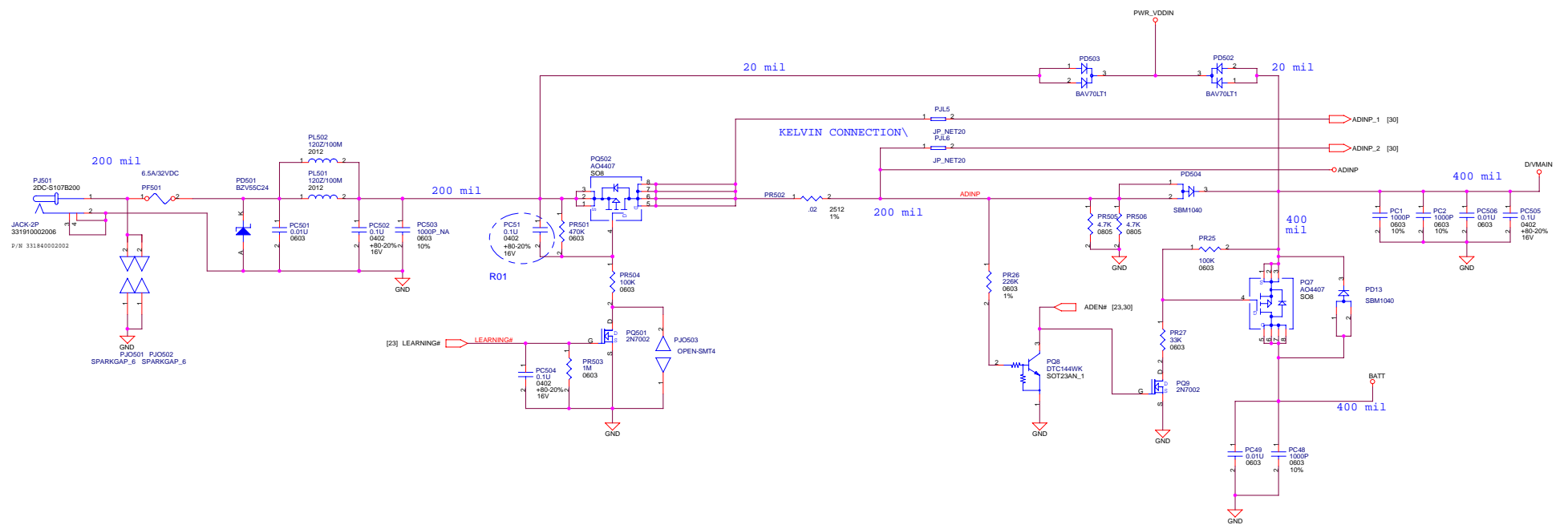
File: KBC (W83L950D)
 Size: 31668520002
 Date: Monday, August 23, 2004
 Sheet: 21 of 30

BIOS / TouchPad / Through Hole

TOUCH PAD

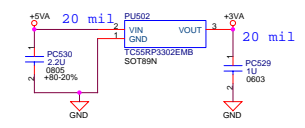
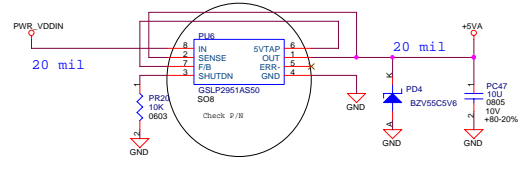
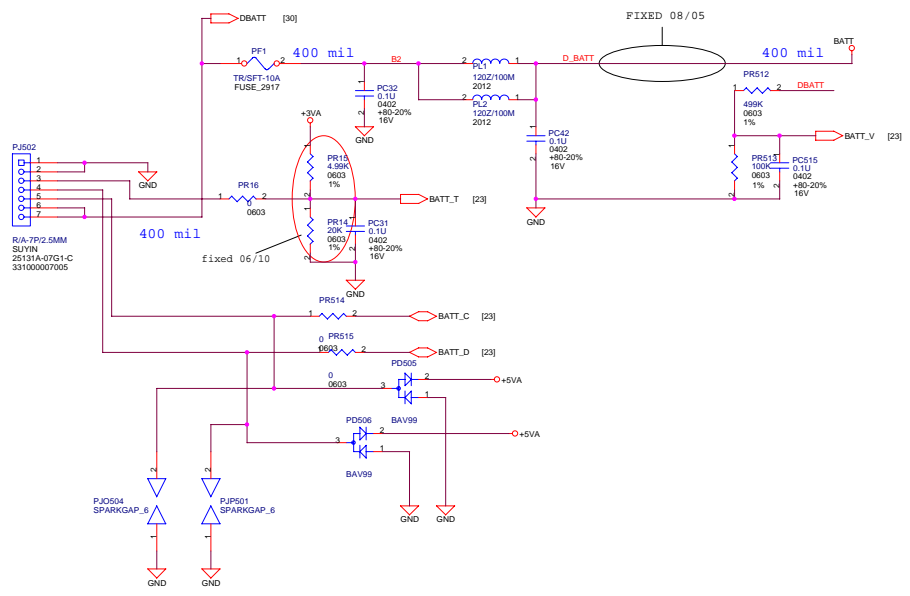


ADP IN / BATT IN / +5VA / +5VAS



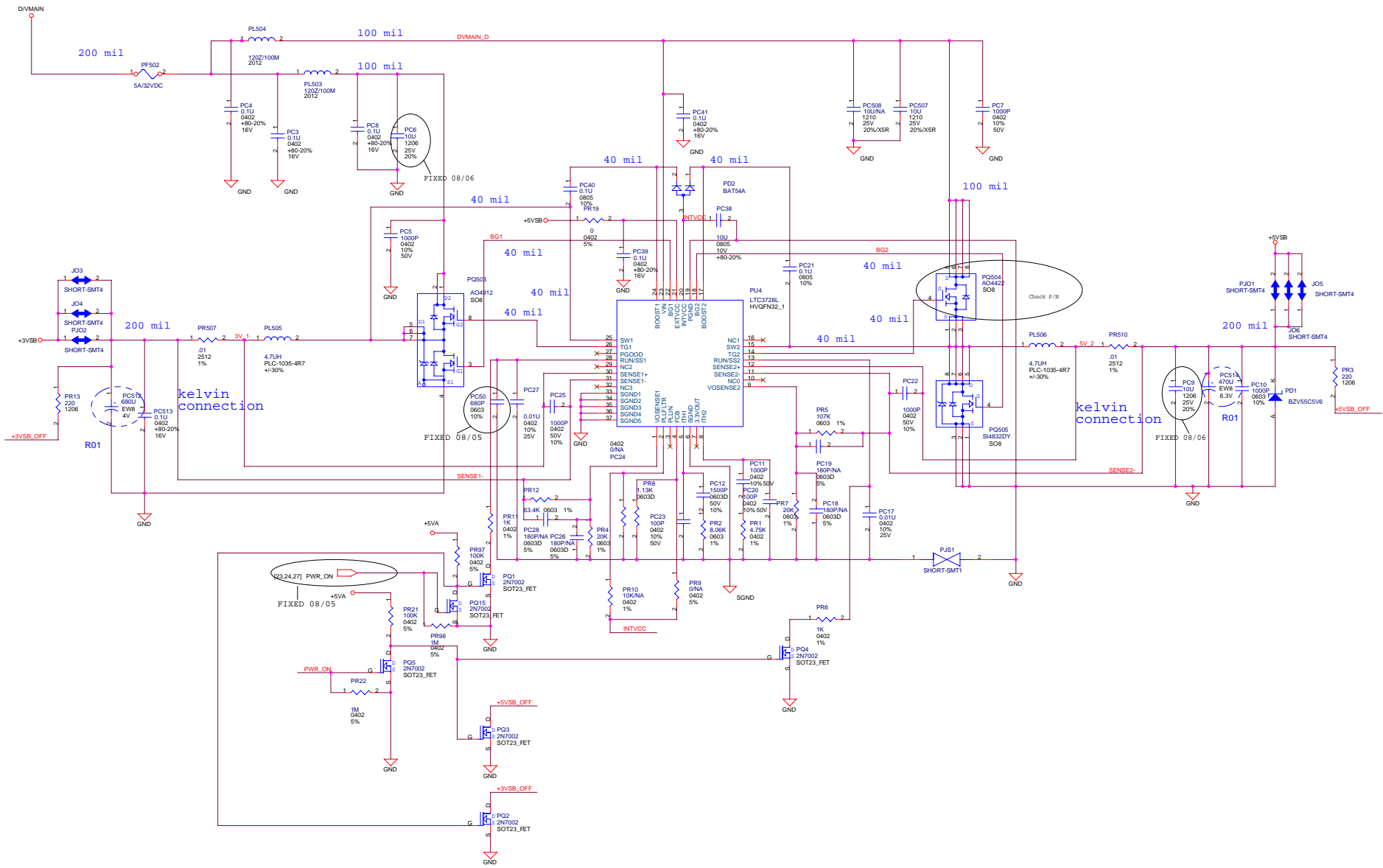
+5VA

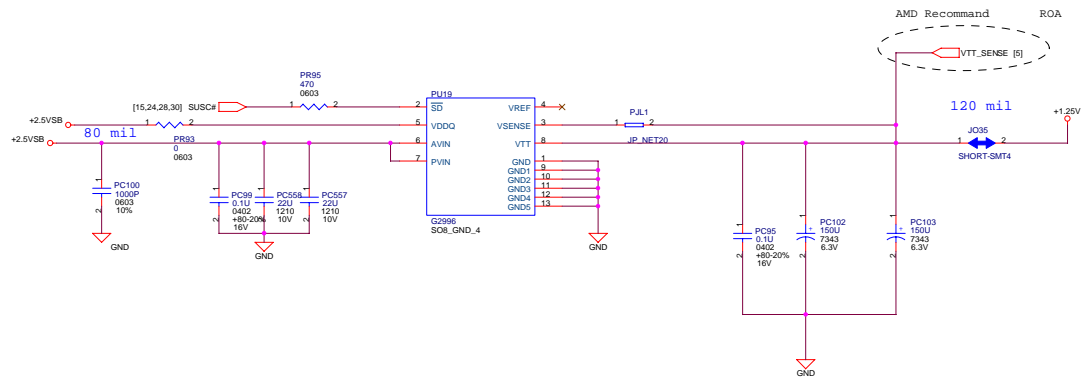
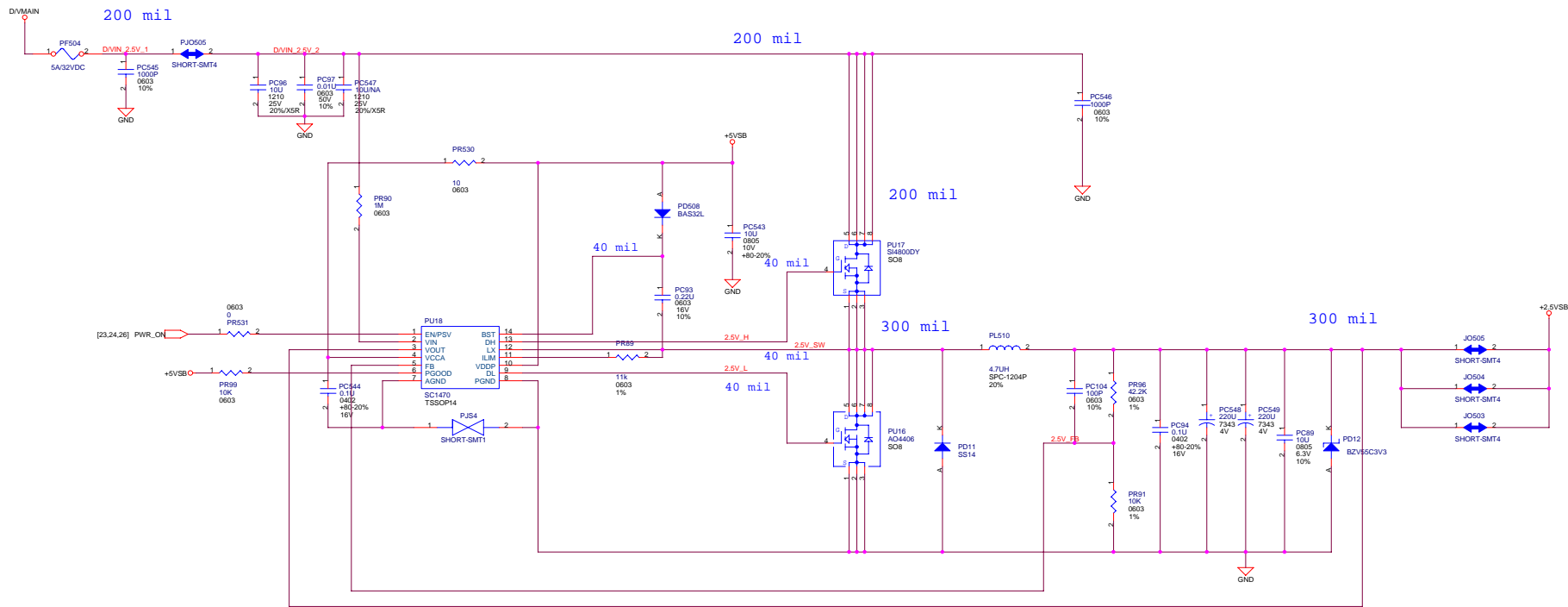
RTC BATTERY



MITAC	
Title ADP IN & BATT IN	
Size Count	Document Number 316684700001
Date	Monday, August 23, 2004
Sheet	25 of 30

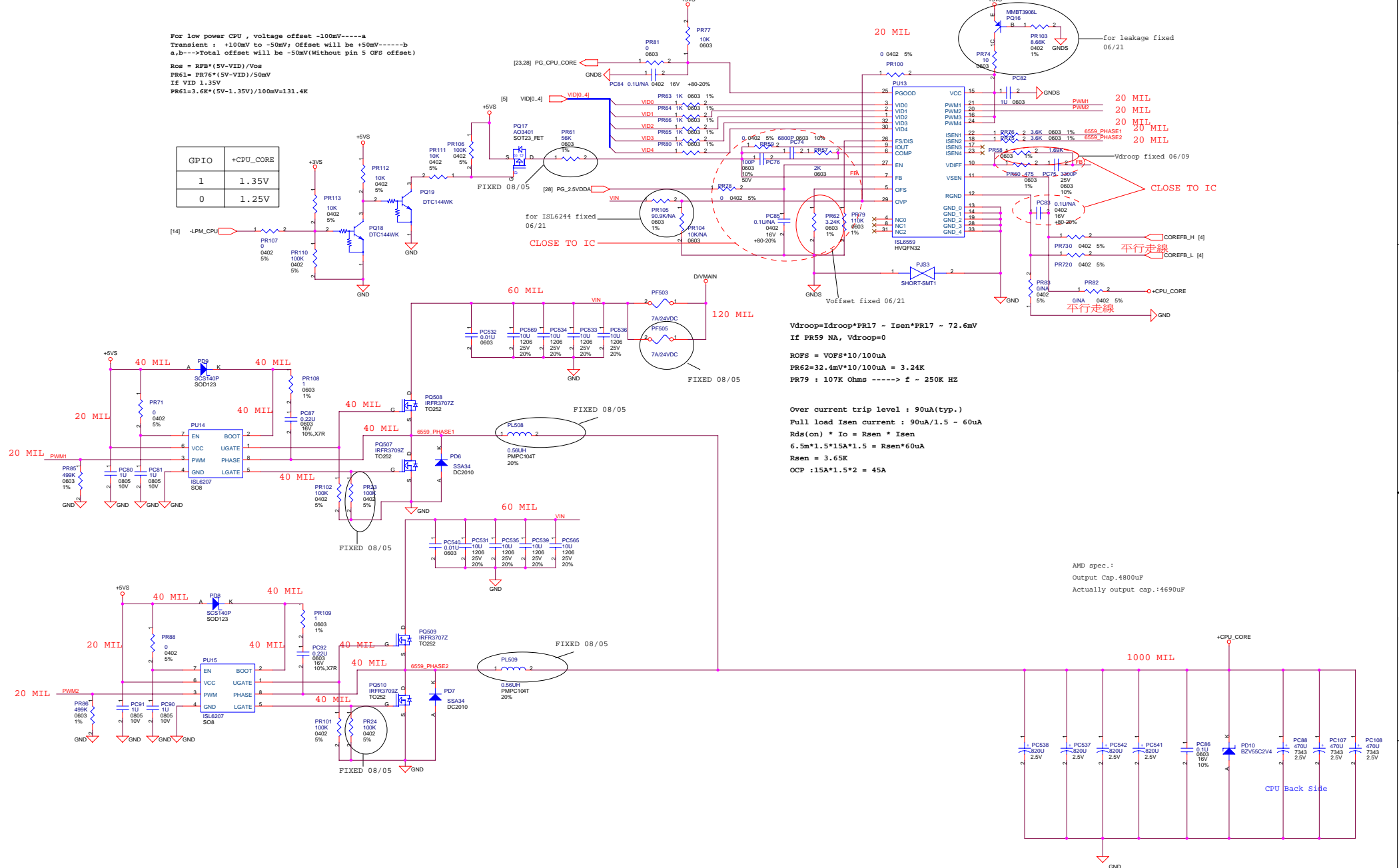
nextint@hotmail.com





For low power CPU , voltage offset -100mV-----a
 Transient : +100mV to -50mV, Offset will be +50mV-----b
 a,b---->Total offset will be -50mV(Without pin 5 OPS offset)
 Ros = RPS*(SV-VID)/Vos
 PR61= PR7*(SV-VID)/50mV
 If VID 1.35V
 PR61=3.6K*(5V-1.35V)/100mV=131.4K

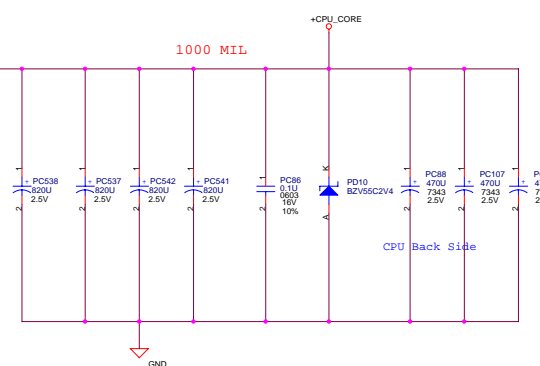
GPIO	+CPU_CORE
1	1.35V
0	1.25V



Vdroop=Idroop*PR17 ~ Isen*PR17 - 72.6mV
 If PR59 NA, Vdroop=0
 ROPS = VOFS*10/100uA
 PR62=32.4mV*10/100uA = 3.24K
 PR79 : 107K Ohms -----> f ~ 250K HZ

Over current trip level : 90uA(typ.)
 Full load Isen current : 90uA/1.5 ~ 60uA
 Rds(on) * Io = Rsen * Isen
 6.5m*1.5*15A*1.5 = Rsen*60uA
 Rsen = 3.65K
 OCP : 15A*1.5*2 = 45A

AMD spec :
 Output Cap.4800uF
 Actually output cap.:4690uF



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